REMARKS

Claim Rejections

In the Final Office Action of June 11, 2003, claims 17-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Marcinkiewicz et al. (U.S. Patent No. 5,422,513) in view of Juskey et al. (U.S. Patent No. 5,371,404).

Drawings

It is noted that no Patent Drawing Review (Form PTO-948) was received with the outstanding Office Action. Thus, Applicant must assume that the drawings are acceptable as filed.

Claims

Claim 17 has been amended to specifically point out that the carrier (220) is made only of metal. Basis for this limitation can readily be found in Applicant's original specification. Specifically, on page 3, lines 13 et seq., it is stated:

> The metal carrier is made of copper, aluminum or other metals...

On page 4 of Applicant's specification, lines 11 et seq., it is stated that:

> The metal carrier 220 is made of copper, aluminum or their alloys...

On page 5, line 25, it is stated:

> Besides, the metal carrier 220 is made of copper, aluminum or other metals...

The only materials disclosed for the carrier layer are metals, namely, copper, copper alloy, aluminum or aluminum alloy. Thus, Applicant submits that the foregoing claim amendments find adequate basis in the original disclosure.

The primary reference to Marcinkiewicz et al. discloses an integrated circuit chip having a substrate (10), a first chip (24), dielectric layers (18) with vias (19) and interconnects (20) formed within the dielectric layers and interconnection pad (22).

On page 3 of the Final Office Action, the Examiner admits that:

> The teaching of Marcinkiewicz et al. as discussed above does not disclose the carrier made of metal or aluminum (re claims17, 25), a plurality of pads formed a grid array (re claims 21, 23), a plurality of connectors such as solder bumps (re claim 22), the dielectric material made of polyimide, epoxy (re claim 24), the conductive column made of aluminum, aluminum alloy, copper, copper alloy (re claim 26).

The cited reference to Juskey et al. discloses a thermally conductive integrated circuit package including a molding compound (20), a semiconductor device (16), an underfill adhesive (25), a substrate (10), a least one conductive via (26) through the substrate.

On page 3 of the Final Office Action, the Examiner states that:

> Re claim 17, 25, Juskey et al disclose a carrier (20) made of metal such as aluminum (col 4, lines 13-15). [Emphasis added].

Applicant respectfully traverses this interpretation of Juskey. Juskey et al. specifically state, at col. 4, lines 5-17:

> The molding compound 20 also encapsulates the underfill material 25 and covers portions or substantially all of the upper surface 15 of the substrate 10. Molding compound 20 comprises a thermally and electrically conductive material, such as an epoxy, having at least one filler, for example, a metallic element or alloy, which substantially contributes to the thermal and electrical conductive properties of the molding compound. The

> molding compound 20 is typically filled to approximately 70% to 75% with copper, aluminum, nickel, gold, silver, or similar type materials to provide electrical and thermal conductivity. [Emphasis added].

Thus, it is clear that the molding compound of Juskey et al. comprises a conductive plastic compound (heat sink) including metal particles, but does not comprise a carrier made only of metal and having a cavity as in Applicant's invention. The molding compound of Juskey et al. (20) is molded and covers the upper surface (15) of the substrate (10). It is abundantly clear that the molding compound (20) is not a carrier for supporting the IC (16) and build-up forming dielectric layers. In addition, the molding compound (20) does not have a top surface coplanar with the active surface of the IC (16) for formation of dielectric layers.

Juskey et al. discloses a metal and plastic molding compound, whereas the present invention discloses a metal carrier. Further, Juskey et al. discloses a single substrate, but does not teach a plurality of dielectric layers formed on the active surface of the die on the top surface of the metal carrier. Additionally, Juskey et al. teaches an underfill adhesive to fill the gap between the semiconductor device and the substrate, but does not teach the die being positioned within the cavity such that the active surface of the die is in coplanar with the top surface of the metal carrier. Further, Juskey et al. teaches at least one conductive via (26) through the substrate, but does not teach each plurality of dielectric layers having a plurality of conductive columns electrically connected to the bonding pads of the die and a plurality of conductive traces electrically connecting corresponding conductive columns of one plurality of dielectric layers to a corresponding conductive columns of another plurality of dielectric layers.

In this particular case, Applicant submits that neither Marcinkiewicz et al., nor Juskey et al contain the slightest suggestion that their respective teachings could be combined as postulated by the Examiner. Absent such a specific teaching in the prior art, there is simply no basis for a rejection under 35 U.S.C. § 103.

Even if the teachings of Marcinkiewicz et al. and Juskey et al. were combined, as suggested by the Examiner, the resultant combination does not suggest a carrier made only of metal and having a cavity in a top surface, the die being positioned within the cavity such that the passive surface and the side are within the cavity.

Summary

In view of the foregoing, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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